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MARTINE & PENILLA, LLP
710 LAKEWAY DRIVE
SUITE 170
SUNNYVALE, CA 94085

EXAMINER	
UMEZ ERONINI, LYNETTE T	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AS

Office Action Summary	Application No.	Applicant(s)	
	09/336,401	SVIRCHEVSKI ET AL.	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 21-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-11, and 21-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This communication is in response to applicants' Remarks (pages 8-9) in the amendment filed January 24, 2004. Applicants' presented persuasive arguments, which show the prior art of record fails to teach an outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer so that the outlet end overlies an edge of the semiconductor wafer. Hence, a new non-final office action is presented.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 4, 5, 6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bersin (US 5,882,489) in view of Tomoeda et al. (US 5,759,614), Gockel et al. (US 5,809,832) and further in view of Tadokoro (US 4,559,718).

As pertaining to claims 1, 5, 6, and 9-11, Bersin teaches a method of cleaning a surface of a semiconductor wafer following a plasma etching operation. The method comprises rinsing the wafer in DI water, optionally with ultrasonic agitation (column 4, lines 22-27), which is the same as using a non-splash rinse technique wherein the non-splash rinse technique being configured to quickly and evenly saturate the surface of the semiconductor wafer.

Bersin differs in failing to teach positioning an outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer so that the outlet end overlies an edge of the semiconductor wafer and wetting the surface of the semiconductor wafer by using a non-plash rinse technique through the outlet end of at least one liquid deliver source, **in claim 1**.

Tomoeda teaches, "The supply nozzle **22** is moved above the center of the wafer W from a waiting position by a moving mechanism (not shown). The rinse solution R is injected (supplied) to the surface of the wafer W rotating in accordance with the driving of the spin chuck **20** at a flow rate of e.g., about 130 cc/min MAX for 1 to 2 seconds . . ." which suggests the outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer so that the outlet end overlies an edge of the semiconductor wafer. Since Tomoeda uses the same method of wetting the semiconductor wafer as in the claimed invention, then using Tomoeda's method in the same manner as the

claimed invention would result the same in wetting the surface of the semiconductor wafer by using a non-plash rinse technique through the outlet end of at least one liquid deliver source.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use Tomoeda's method of wetting a wafer for the purpose of uniformly removing unwanted material from the entire wafer surface.

Bersin in view of Tomoeda differs in failing to teach scrubbing the surface of the semiconductor wafer with a cleaning brush that applies a chemical solution to the surface of the wafer, **in claim 1** and wetting and scrubbing in a brush box, **in claim 4**.

Gockel teaches, "A wet processing system such as the scrubber described above comprises several distinct stations or modules. Each module is typically enclosed in a box-like structure, which comprises the appropriate processing apparatus for that station. For example, a scrubber may comprise a load or send station, one or more scrub stations, a spin rinse and spin dry station, . . ." (column 1, lines 21-28). "A scrub station typically comprises one or more brushes, . . . during scrubbing and sprays or nozzles for dispensing chemicals" (column 1, lines 39-42). "Each brush includes multiple protrusions . . . to facilitate the cleaning of wafers . . . the upper and lower brushes are configured to provide fluid (same as chemical) to the core of the brush to be dispersed to the . . . brush surface," (column 8, lines 13-17). The aforementioned, reads on, scrubbing the surface of a wafer with a cleaning brush that applies a chemical solution to the surface of the wafer after the wetting, as in claim 1. Gockel further

teaches, "In brush **1** station **1420**, a dirty wafer **1402**, is brushed and sprayed . . ." (column 15, lines 3-6) and " . . . incorporating spray heads **505** and **506** to spray cleaning solutions . . . onto the wafer . . ." (column 7, lines 50-53 and Figure **5**), which reads on setting a first delivery and a second delivery source over the surface of the wafer in order to wet the surface of the wafer with a flow rate of water and further reads on, performing the wetting and scrubbing in a brush box, as **in claim 4**.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bersin in view of Tomoeda by using the scrubbing method as taught by Gockel for the purpose of removing wafer contaminants that may cause device failure to occur at a faster rates than usual (Gockel, column 1, lines 11-13).

Bersin in view of Tomoeda and Gockel differs in failing to teach keeping the wafer substantially dry, **in claim 1**.

Tadokoro teaches, " . . . a method . . . for drying a semiconductor wafer, is capable of drying the wafers in a perfect manner while keeping them clean, thereby enhancing the quality of the dried wafers" (column 1, lines 32-36), which reads on keeping the semiconductor wafer substantially dry.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Bersin in view of Tomoeda and Gockel by using Tadokoro's method of drying a semiconductor wafer for the purpose of enhancing the quality of dried wafers (Tadokoro, column 1, lines 32-36).

Bersin in view of Tomoeda, Gockel, and Tadokoro differs in failing to teach rotating the semiconductor wafer about a radial axis at a rate of between about 2 revolutions per minute and about 20 revolutions per minute, **in claim 8**.

It is would have been obvious to one having ordinary skill at the time of the claimed invention to select any range of rotational rates of semiconductor wafers as taught by the references, including specifically range (rotational rates) as claimed by applicants for the purpose of uniformly processing the wafer surface the same.

4. Claims 21-24 rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (US 5,804,091) in view of Tomoeda (US '489) Gockel (US '832), and further in view of Elliott et al. (US 5,669,979)

As pertaining to claim 21, Lo teaches a method of cleaning a surface of a semiconductor wafer following a plasma etching operation. The cleaning method comprises: water flushing with megasonic shaking to clean the wafer surface (Abstract; column 1, lines 39-52; column 2, lines 3-34; column 7, lines 50-53 and Figure **5**), which is the same as wetting the surface of the semiconductor wafer by using a non-splash rinse technique. Using Lo's method of cleaning a wafer surface in the same manner as the claimed invention would result in the non-splash rinse technique being configured to quickly and evenly saturate the surface of the semiconductor wafer. Lo's method further reads on, applying liquid to the surface of the semiconductor wafer through the outlet end of the at least one delivery source. Lo's plasma etching operation is described as a conventional process that is used in making tungsten plug (column 1, lines 13-36) and

is called tungsten etch back (column 2, lines -13), which is the same as the plasma etching operation is a tungsten etch-Back (WEB) operation, **as in claim 24**.

Lo differs in failing to teach setting an outlet end of at least one delivery source over the surface of the semiconductor wafer, **in claim 21**.

Tomoeda teaches, "The supply nozzle **22** is moved above the center of the wafer W from a waiting position by a moving mechanism (not shown). The rinse solution R is injected (supplied) to the surface of the wafer W rotating in accordance with the driving of the spin chuck **20** at a flow rate of e.g., about 130 cc/min MAX for 1 to 2 seconds . . .," which suggests the outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer so that the outlet end overlies an edge of the semiconductor wafer. Since Tomoeda uses the same method of wetting the semiconductor wafer as in the claimed invention, then using Tomoeda's method in the same manner as the claimed invention would result the same in wetting the surface of the semiconductor wafer by using a non-plash rinse technique through the outlet end of at least one liquid deliver source.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Lo by using Tomoeda's method of wetting a wafer for the purpose of uniformly removing unwanted material from the entire wafer surface.

Lo in view of Tomoeda differs in failing to teach setting an outlet end of at least one delivery source over the surface of the semiconductor wafer at an angle in a range from about 5 degrees to about 35 degrees relative to the surface of the wafer, **in claim**

21; setting the outlet end of the at least one delivery source to overlie and edge of the semiconductor wafer by a distance in a range form about 2 mm to about 30 mm, **in claim 22**; and applying deionized wafer at a flow rate between 50ml/minute and about 300 ml/minute, **in claim 23**.

Elliott teaches a method of cleaning a surface and the depth of substrate surface below the surface of the liquid may be less than 50 mm, and preferably less than 20 mm (column 2, lines 13-15), which lies within applicant's range from 2 mm to about 30 mm. The fluid may be a gas or liquid directed at an angle of less than 90 degrees to the surface, preferably between 0 and 20 degrees (column 2, lines 18-21 and 27-30), which falls within applicant's range from about 5 to 35 degrees. Elliott also teaches surface cleaning semiconductor substrate using a liquid that has a velocity between 0.2 mm/sec and 2,000 mm/sec (column 1, lines 11-25 and column 2, lines 9-12 and 28-30). Elliot's flow rate, which is reported in terms of a velocity, provides evidence that the flow rate as well as the range of the angle at which the fluid (delivery source) is directed to the wafer surface and range of distance at which the fluid (delivery source) overlies the wafer, area so-called "result effective variables."

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Lo in view of Tomoeda by employing using Elliott's angles, depths, and flow rates, which have been shown to be a so-called "result effective variable," since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Lo in view of Tomoeda and Elliott differs in failing to teach scrubbing the surface of the semiconductor wafer with a cleaning brush that applies a chemical solution to the surface of the wafer, **in claim 21**

Gockel teaches, "A scrub station typically comprises one or more brushes, . . . during scrubbing and spray or nozzles for dispensing chemicals" (column 1, lines 39-42).

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Lo in view of Tomoeda and Elliott by using the scrubbing method as taught by Gockel for the purpose of removing wafer contaminants that may cause device failure (Gockel, column 1, lines 11-13).

5. Claims 25-27 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gockel (US '832) in view of Tomoeda (US '619) and Tadokoro (US '718) and further in view of Elliott (US '979).

Gockel teaches a method for cleaning the surface of semiconductor wafers. The method comprises: loading and moving dirty wafers from load station to from load station to scrubber (column 14, lines 60-64 and Figure **14)**, which reads on,

receiving a semiconductor wafer.

Gockel teaches, incorporating spray heads **505 and 506** that are mounted at the entrance and exit of brush boxes **105 and 106** to spray cleaning solution onto wafers (column 7, lines 51-53 and Figure **5**), which reads on,

positioning an outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer and applying liquid to the surface of the semiconductor wafer through the outlet end of the at least one liquid delivery source.

Gockel differs in failing to teach positioning an outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer so that the outlet end overlies an edge of the semiconductor wafer, **in claim 25**.

Tomoeda teaches, "The supply nozzle **22** is moved above the center of the wafer W from a waiting position by a moving mechanism (not shown). The rinse solution R is injected (supplied) to the surface of the wafer W rotating in accordance with the driving of the spin chuck **20** at a flow rate of e.g., about 130 cc/min MAX for 1 to 2 seconds . . .," which suggests the outlet end of at least one liquid delivery source relative to a surface of the semiconductor wafer so that the outlet end overlies an edge of the semiconductor wafer. Since Tomoeda uses the same method of wetting the semiconductor wafer as in the claimed invention, then using Tomoeda's method would result the same in wetting the surface of the semiconductor wafer by using a non-plash rinse technique through the outlet end of at least one liquid deliver source.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Gockel by using Tomoeda's method of wetting a wafer for the purpose of uniformly removing unwanted material from the entire wafer surface.

Gockel in view of Tomoeda differs in failing to teach, the semiconductor wafer being substantially dry.

Tadokoro teaches, "a method . . . for drying a semiconductor wafer, which is capable of drying the wafers in a perfect manner while keeping them clean, thereby enhancing the quality of the dried wafers" (column 1, lines 32-36), which reads on keeping the semiconductor wafer substantially dry.

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Gockel in view of Tomoeda by using Tadokoro's method of drying a semiconductor wafer for the purpose of enhancing the quality of the dried wafers (Tadokoro, column 1, lines 32-36).

Gockel in view of Tomoeda and Tadokoro differs in failing to teach specify processing variables such as a distance from about 2 mm to about 30 mm from where the delivery source overlies an edge of the semiconductor wafer; an angle in a range from 5-35 degrees of the outlet end of the liquid delivery source relative to the wafer surface, the distance of 2 to 15 mm from where the outlet end is disposed above the surface of the semiconductor wafer, **in claims 25**; flow rate between 50 ml/minute and 300 ml/minute through the outlet end of the liquid delivery source, **in claim 27**; a distance from about 5 mm from the outlet end of the delivery source that overlies an edge of the semiconductor wafer, **in claim 29**; an angle of 15 degrees is oriented from the outlet end of the delivery source relative to the surface of the semiconductor wafer,

in claim 30; and a distance about 7 mm from outlet end of the delivery source that is disposed above the surface of the semiconductor wafer, **in claim 31**.

Elliott teaches the depth of substrate surface below the surface of the liquid may be less than 50 mm, and preferably less than 20 mm (column 2, lines 13-15), which lies within applicant's range from 2 mm to about 30 mm. The fluid may be a gas or liquid directed at an angle of less than 90 degrees to the surface, preferably between 0 and 20 degrees (column 2, lines 18-21 and 27-30), which falls within 5 to 35 degrees, as in the claimed invention. Elliot also teaches surface cleaning semiconductor substrate using a liquid that has a velocity between 0.2 mm/sec and 2,000 mm/sec (column 1, lines 11-25 and column 2, lines 9-12 and 28-30). Elliott's flow rate, which is reported in terms of a velocity, provides evidence that the flow rate as well as the range of the angle at which the fluid (delivery source) is directed to the wafer surface and the range of distance at which the fluid (delivery source) overlies the wafer, are so-called "result effective variables."

It is the examiner's position that it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Gockel in view of Tomoeda and Tadokoro by employing using Elliott's angles, depths, and flow rates, which have been shown to be a so-called "result effective variable," since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gockel (US '832) in view of Tomoeda ('614), Tadokoro (US '718) and Elliott (US '979) as applied to claim 25 above.

Gockel in view of Tomoeda, Tadokoro and Elliot differ in failing to teach the semiconductor is rotated about a radial axis at a rate of about 2 revolutions per minute to about 20 revolutions per minute.

It is would have been obvious to one having ordinary skill at the time of the claimed invention to select any range of rotational rates of semiconductor wafers as taught by the references, including specifically range (rotational rates) as claimed by applicants for the purpose of uniformly processing the entire wafer surface.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 4-11, and 21-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ltue

May 13, 2004

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER